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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/734,656	12/15/2003	Masahiro Owada	016907-1587	8983

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FOLEY AND LARDNER
SUITE 500
3000 K STREET NW
WASHINGTON, DC 20007

EXAMINER	
PAREKH, NITIN	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 01/21/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

H·A

Office Action Summary	Application No.	Applicant(s)	
	10/734,656	OWADA, MASAHIRO	
	Examiner	Art Unit	
	Nitin Parekh	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☒ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 2.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

2. Claims 3 and 9 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

A. Claim limitations as recited in claims 3 and 9, line 2, include "the wiring layer having a width which is greater than a minimum wiring width prescribed by design rules".

However, the description in the specification does not include a value of the minimum wiring width prescribed by design rules.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-11, insofar as being in compliance with 35 U.S.C. 112, are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakamura (US Pat.6166442) in view of Tsubouchi et al. (US Pat. 5208187).

Regarding claims 1, 2 and 4-6, Nakamura discloses a semiconductor device comprising:

- an aluminum wiring layer having a width of 5 microns or greater than 5 microns (see 11 in Fig. 1; Col. 2, lines 55-65) having a plurality of divided wirings (see 14 in Fig. 1) extending a predetermined direction/first direction, the plurality of divided wirings being divided from each other in a direction perpendicular to the extending direction (see Fig. 1)
- the divided wirings each having a width of about 2 microns or less, or 1.44 microns (Col. 2, line 65- Col. 3, line 40), and
- a plurality slit-shaped non-wiring layers/insulation layers comprising an oxide and silicon nitride (see 13 in Fig. 1- not explicitly shown in a cross-sectional view; see Col. 3, lines 1-14), each which is formed between the plurality of divided wirings of the wiring layer at predetermined intervals in a second direction perpendicular the first direction, the non-wiring layers extending in the extending direction of the plurality the divided wirings

(Fig. 1; Fig. 1-5; Col. 1-4).

Nakamura fails to teach:

- the wiring layer being formed on a semiconductor substrate, and
- the wiring layer being formed of a plurality of grains and the divided wirings each having a width smaller than a size of the grains.

Tsubouchi et al. teach an aluminum metallization structure in a device, the structure comprising:

- the metallization being conventionally formed on a substrate or underlying insulating layers/first insulating layer (see metal layers 3, 4, 6, 7, etc. on the insulating films 2, 5, etc. in Fig. 1A-2C; Col. 5-7), and
- the aluminum/aluminum alloy wiring layer (Col. 7, lines 1-35; Col. 5-7) being formed such that a width/L1 of the wiring ranges from 0.5-20 microns including that as small as 0.5 microns (see L1 in Fig. 2A; Col. 7, lines 11-35; Col. 12, line 15), and
- the wiring layer being formed of a plurality of grains where the size of the grains is in a range of several microns to 10 microns (Col. 12, line 38- Col. 14, line 27; Fig. 2A; Fig. 15A), such aluminum metallization structure providing improvement in electromigration resistance and stress reduction (Col. 3; Col. 12-14).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the wiring layer being formed on a semiconductor

substrate and the wiring layer being formed of a plurality of grains such that the divided wirings each having a width smaller than a size of the grains as taught by Tsubouchi et al. so that the electromigration resistance can be improved and the stress can be reduced in Nakamura's device.

Regarding claim 3, Nakamura and Tsubouchi et al. teach the entire claimed structure as applied to claim 1 above, except the wiring layer having a width being greater than minimum wiring width prescribed by design rules.

The determination of parameters such as wiring length/width, thickness/depth, number of such layers, width/thickness of an insulating layer, number of insulating layers, dimension of split/aperture in the wiring g layer, etc. in multilevel metallization and interconnect technology art is a subject of routine experimentation and optimization to achieve the desired bonding strength, reduced level of metallization defects such as crack/void formation, lift-off, etc., reduced thermal stress, and improved reliability.

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the wiring layer having a width being greater than minimum wiring width prescribed by design rules so that the stress can be reduced and the reliability can be improved in Nakamura's device.

Regarding claims 7, 8, 10 and 11, Nakamura and Tsubouchi et al. teach the entire claimed structure as applied to claims 1, 2, 4 and 6 above.

Regarding claim 9, Nakamura and Tsubouchi et al. teach the entire claimed structure as applied to claims 7, 1 and 3 above.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nitin Parekh whose telephone number is 571-272-1663. The examiner can normally be reached on 09:00AM-05:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on 571-272-1732. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9318.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

Nitin Parekh

NP

01-20-05

NITIN PAREKH

PRIMARY EXAMINER

TECHNOLOGY CENTER 2800